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Experimental Investigation of a Linear 500-Element 3-Phase Charge-Coupled Device

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A linear, 500-element, 3-phase charge-coupled device, originally built as a high-resolution linear image sensor, has been chosen as a representative structure for single-level, 3-phase charge-coupled devices to exemplify the performance of such devices in detail.

Charge-handling ability and transfer efficiency have been studied as a function of various design parameters and operating conditions. Most of the observed functional dependences are well understood and agree with the expectations based on model calculations. However, various problems are encountered in these structures. An unusually wide spread of the performance of different devices and slow instabilities are observed. They are attributed to a lack of control of the interface potential in the gaps between the transfer electrodes.

Some emphasis is placed on a more detailed description of the various measurement techniques used. These techniques are of a general interest since they are applicable to other charge-transfer devices.

I. INTRODUCTION

The principle of charge coupling was first conceived using a 3-phase technique with simple, nondirectional transfer electrodes.[1] This approach using all identical electrodes in a single level of metallization has been successfully demonstrated on several successive designs of linear devices; each structure has a greater number of elements with smaller electrode length than the previous design.[2–4] Correspondingly, improved efficiency at higher frequencies has been observed.

The charge-coupled device (CCD) discussed in this paper was designed as a high-resolution linear image sensor with 500 three-phase elements at a spatial period of 18 μm, capable of reading half a line of

a normal page of printed material.[4] The device has also been demonstrated as an analog shift register able to delay a line of the *Picturephone*® video signal.[5] In these demonstrations, a few of the best devices have been used, and their performance has been described in the context of these particular demonstrations only. The following discussion enlarges the description of the performance of 3-phase single-level metal CCD's by reporting more representative results obtained in a study of many devices. The goal of this study was to obtain an understanding of the functional dependences of charge-handling ability, transfer efficiency, and dark current on operating potentials, frequency, and temperature. In addition, devices with different electrode lengths and different fabrication technologies have been compared. However, similar devices on different slices show a wide performance spread and slow instabilities and show that some results are even irreproducible. All this is attributed to a lack of control of the interface potential in the gaps between the transfer electrodes.

The techniques used to determine signal-handling ability, transfer efficiency, or dark current profiles are described in some detail, since they are applicable to the investigation of other charge-transfer devices.

II. THE 500-ELEMENT DEVICE

The device discussed in this paper was designed as a linear image sensor with high-resolution density. At the same time, the device was supposed to serve as a test structure for the high-frequency performance of 3-phase CCD's. To obtain good transfer efficiency, a "smooth" interface potential profile with no barriers or pockets is required, which transfers the minority carriers under the influence of electric fringe fields from electrode to electrode. Extensive computer modeling studies[6] have shown that this condition can be achieved in a 5×10^{14} cm^{-3} silicon substrate with 3000 Å of SiO_2 as an insulator and electrodes shorter than 5 μm. If, in addition, the gaps between the electrodes are made 3 μm or smaller, the device can be operated at pulse amplitudes of 15 V and no barriers will form underneath the transfer gaps for charge densities at the Si-SiO_2 interface ranging from about 5×10^{10} to 2×10^{11} cm^{-2}. Thus, the unit cell was made as small as possible using available technology. Individual electrodes, nominally 3 μm long, were arranged at a spatial period of 6 μm, leading to a cell length of 18 μm. The calculated transfer time constant for electrons lies in the subnanosecond range. Ideally, the transfer efficiency in the frequency range of this study should then be limited by the effects of

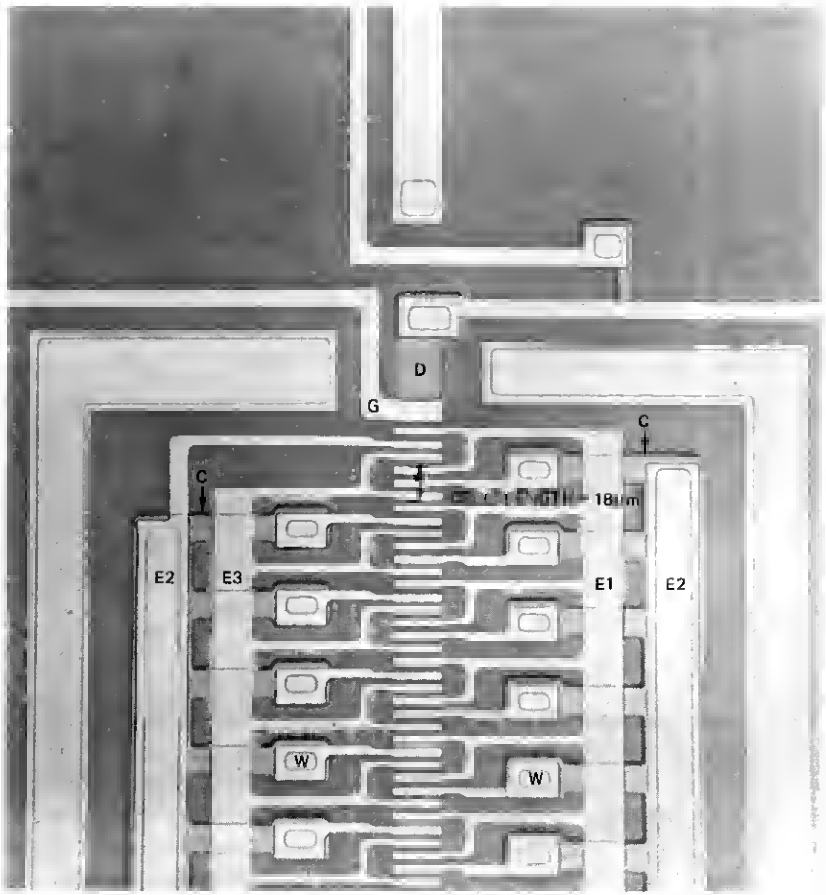

Fig. 1—One end of the linear 500-element 3-phase CCD. Shown are the three sets of transfer electrodes (E1, E2, and E3), the input diode (D), and the input gate (G). Electrodes E2 are alternately contacted to diffused crossunders (C) through contact windows (W) lying on either side of the transfer channel.

interface states. This was indeed found true for the best devices, which showed no problems associated with the bare transfer gaps.

A 3-phase CCD needs one crossing of electrodes per element, which in this device are realized with diffused crossunders. They are introduced by the same phosphorous diffusion (10^{18} cm^{-3}) that forms the input output diodes. The crossunder bus line that addresses electrode system $E2$ (Fig. 1) is repeated on either side of the transfer channel, and the transfer electrodes $E2$ in subsequent elements are contacted

alternately to either one of tbem. In the resulting structure (Fig. 1), which has a periodicity corresponding to two CCD elements, considerably larger and tbus more reliable contact windows can be formed tban in a conventional approacb witb only one bus line.

The channel width, defined by a channel-stopping boron diffusion (10^{17} cm^{-3}), was designed to be 15 μm, taking into account a lateral diffusion of 1.5 μm. This widtb was chosen as a compromise between tbe preference for higher signal levels and the reduction in tbe vertical resolution that would be caused by too wide a channel if tbe device is used as a line scanner with no separate means to restrict the light-sensitive area.

Tbe transfer channel is terminated at both ends by input output diodes. They are electrostatically shielded from the pulsed transfer electrodes by a gate electrode, which in normal operation is kept at a dc potential. Thc wbole device is surrounded by large substrate contacts which servc as points of reference for tbc driving pulses. A special small substrate contact near the output diode can serve as a reference ground for thc video signal. Including tbese features, the device dimensions are 230 μm $\times$ 9150 μm.

Devices were fabricated originally on 10-ohm-cm p-type silicon substrates, witb 3000 Å of SiO_2. Devices with 1500 Å of SiO_2, or witb a double insulator structure consisting of 1200 Å of SiO_2 and 500 Å of Al_2O_3, were also built for comparison.

In most devicos, the transfer electrodes were chemically etched out of 1500 Å of RF-diode sputtered tungsten. Some batches, bowever, used Al or backsputter delineated[7] Ti-Pd-Ni metallization. With two sets of masks, various exposure times of the photoresist, and various etching procedures, the electrode length could be varied in different batches from about 1.5 μm to 4.5 μm. After metallization, the devices were subjected to annealing treatments to reduce tbe interface state density. Most commonly, the devices witb refractory electrodes were beated in a hydrogen atmosphere at 700°C for 1 hour; the Al devices were annealed at 380°C. A considerable improvement in transfer efficiency was normally observed.

In operation, many devices sbowed a strong sensitivity to changes of the ambient, whicb could be demonstrated by breathing onto the surface. To reduce these effects, some devices were protected witb a second dielectric level, such as 1 μm of a phosphorous glass or 1000 Å silicon nitride.

Most of the results presented in tbe following sections were obtained on devices with 3000 Å of SiO_2, with electrodes 3.5 μm long of RF-

diode sputtered tungsten, and with no protective dieleetric layer on top of the electrodes. Deviations in hehavior due to different technologies will be discussed in a special section.

III. EXPERIMENTAL PROCEDURE

After screening tests on the uncut wafer, working devices were mounted on ceramic substrates for the investigation. A few selected devices have been demonstrated as line image sensors[4] or analog delay lines.[5] The following sections present a detailed report of studies carried out on several different devices with reasonably good performance.

The mounted devices were investigated in a test setup, illustrated in Fig. 2, built around an optical microscope. A set of TTL logic, three sets of pulse drivers with different rise times, and several preamplifiers with various handwidths were used to investigate the devices in the frequency range from 1 kHz to 17 MHz. The devices could be operated

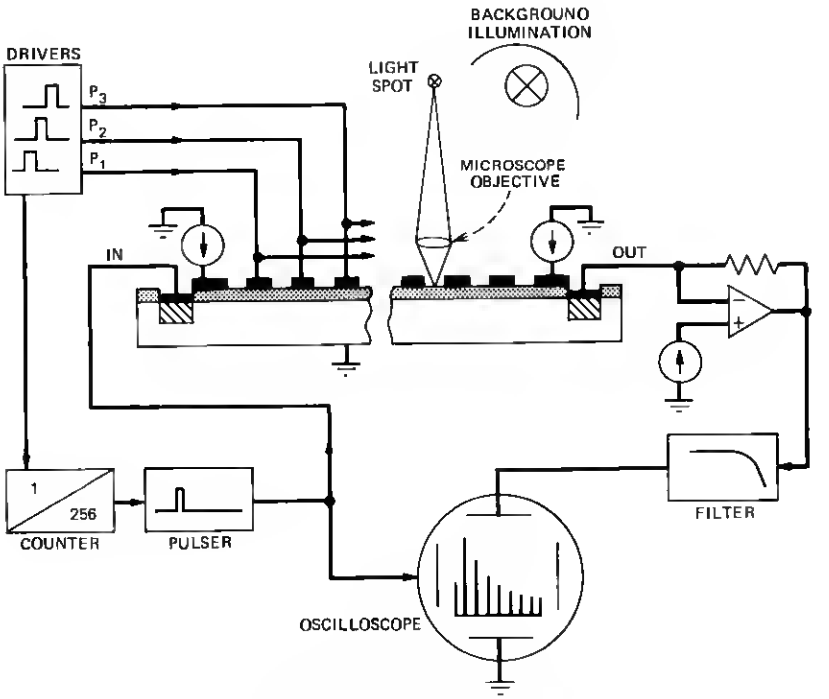

Fig. 2—Schematic layout of test setup.

as analog shift registers with tbe driving pulses applied continuously and charge packets injected periodically througb tbe input diode. Alternatively, the devices could be held in the storage mode, integrating the dark current or carriers generated by light projeeted onto it. A sbarp spot of ligbt, about 2 μm in diameter, projected through the microscope, was especially useful in tbese investigations. By moving the spot along the device, singularities in transfer bebavior could be localized and often associated with visually observable defects. Tbe built-in object illumination of tbe microscope was used in addition to provide a fairly uniform background.

Tbe accumulated charge could be read out at various clock rates after various integration times. The driving pulse shapes, pulse amplitudes, and bias potentials, and the mutual overlap between subsequent pulses could also be varied to study their effects on tbe performance of each device.

IV. CHARGE HANDLING

The basic task of any charge-transfer device is to carry charge along tbe transfer cbannel. An important characterization of a device is, tberefore, the maximum amount of charge that can be handled at a given amplitude of the driving pulses. In the following section, the functional dependence of the charge handling ability on various operating parameters will be investigated.

The maximum amount of charge that can be carried in the potential wells underneath the transfer electrodes for a given set of operating conditions is measured by observing the output signal as tbe device is driven into saturation. In the shift-register mode this can be achieved electrically by injecting more and more charge from the input diode. In the storage mode a light spot is used to fill a single well until it starts to spill into neighboring elements. In both cases, beyond saturation tbe output signal pulse starts to widen rapidly and its amplitude increases only slowly and often in an irregular manner.

The amount of cbarge that a transfer pad can bold is approximately determined by the product of the oxide capacitance underneath the pad C_{ox} and the applied voltage $V_R + V_P$. Fringe effects increase that capacitance somewhat. On the other band, not all tbe applied voltage will appear across the oxide. The interface potential for a full bucket will still be larger than zero. In fact, it cannot be lower than the barriers produced by the isolating electrodes, which are kept at a voltage V_R, without spilling cbarge. Neglecting fringe effects and the influence of tbe depletion capacitance, one expects a linear relationship

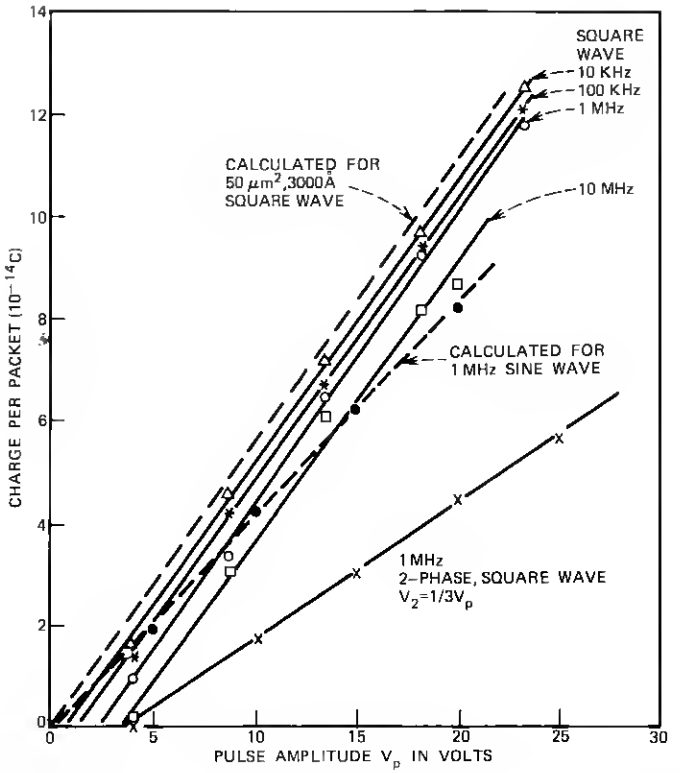

Fig. 3—Charge-handling ability as a function of applied pulse amplitudes for various waveforms.

between the driving pulse amplitude V_P and the signal-handling ability: $Q = C_{ox} \cdot V_P$.

Experimental results derived from the saturation value of the output signal show good agreement with this approximation (Fig. 3). For ordinary 3-phase operation with square pulses, the slope of the curves corresponds to an electrode capacitance of 5.6×10^{-15} F, which in turn corresponds to an area of 50 μm^2 on 3000 Å of SiO_2. With a channel width of 15 μm, this yields a calculated effective electrode length of 3.3 μm, which agrees with the observed length within the measurement accuracy of 0.5 μm.

Curves taken at various pulse rates are parallel but do not fall on top of each other. Somewhat lower charge handling is observed as the frequency increases, and the corresponding extrapolated curves cross the abscissa at higher values of V_P. Comparison of measurements

taken at a fixed clock rate but with pulses that have a different fall time show reduced signal amplitude for the slower pulses. This indicates that the frequency dependence of the charge-handling ability may originate from the degradation of the driving pulses. Stray capacitance and the resistance of the diffused crossunders slow down the response time and reduce the pulse amplitude at higher frequencies.

The device was also operated with sine waves and the maximum signal charge plotted as a function of peak-to-peak amplitude. The expected values in this mode are 75 percent of the square-wave operation, since, when one phase is at its maximum value V_P, the two neighbors are at a voltage $V_P(1 + \cos 120°)/2 = 0.25\ V_P$. Experimentally observed values fall well upon the calculated straight line through the origin. These measurements show a much smaller frequency dependence.

A 3-phase device can also be operated in an asymmetric 2-phase mode hy leaving one set of electrodes at an intermediate dc potential V_2. Using a simplistic model that neglects fringe effects, one would

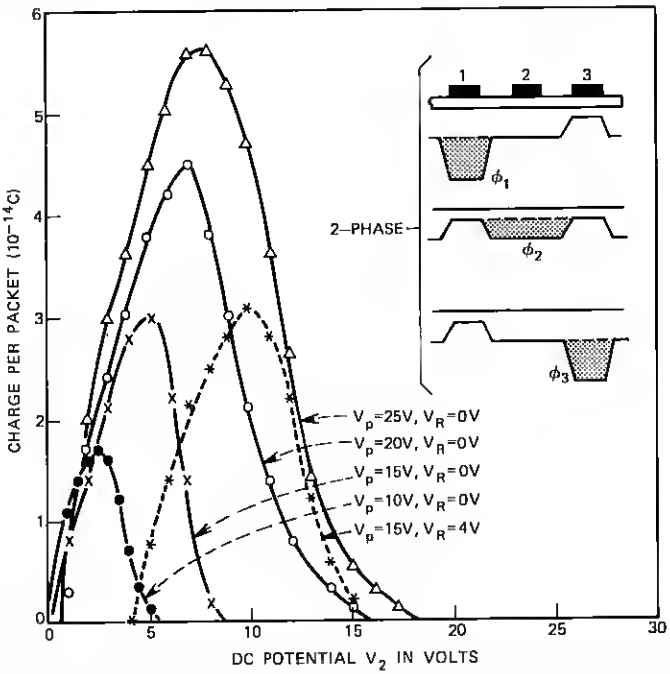

Fig. 4—Charge-handling ability in asymmetric 2-phase mode of operation (see inset) as a function of the dc potential of the static phase for various pulse amplitudes.

expect that the largest signal current could he carried when this intermediate potential V_2 is at half the pulse voltage V_P, and that for this case the signal handling should be half that of the normal 3-phase operation.

Experimentally, it is seen that for all measured values of V_P, the maximum signal current is reached for a dc potential V_2 equal to about one-third of V_P (Fig. 4). For this case, the charge-handling ability is ahout 40 percent of that ohserved in normal 3-phase operation. This is due in part to the fact that for higher values of V_2 the transfer efficiency dccreases, owing to the formation of insuppressihle harriers hctween the dc phase and an adjacent phase that is fully turned on. Also, in this structure that has gap widths comparahle to the electrode lengths, the gaps themselves may play a significant role in the charge-storage process. The inset of Fig. 4 illustrates that fact. In this model the dc phase V_2 turned on to $V_P/3$, together with the two adjacent gaps, can store the same amount of charge as the well underneath phase 1 or 3 in the asymmetric 2-phase mode.

The important role of the potential in the gaps is also expressed in a strong dependence of the performance on the resting potential V_R. The inset of Fig. 5 shows the function of V_R serving as a hias on top

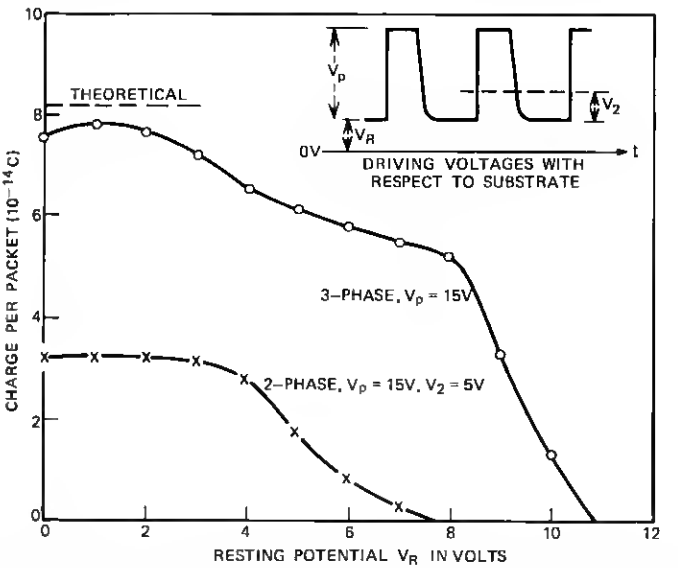

Fig. 5—Charge-handling ability as a function of resting potential V_R (see inset for definition) for normal 3-phase operation and for the asymmetric 2-phase mode.

of which the pulse potentials and, if applicable, V_2 are floating. Figure 5 then shows the dependence of the charge-handling ability on the rest potential V_R. In the normal 3-phase mode, the operating range of V_R is about 8 V. This is a rather high value for a 3-phase CCD. Typically, these devices are much more sensitive to V_R and show ranges of only 1 to 3 V. The range of V_R increases for higher pulse voltages V_P, because the stronger fringe fields can suppress larger barriers in the gap. In the asymmetrical 2-phase mode, where the voltage difference on adjacent pads is smaller, a smaller operating range of V_R is found.

Switching all electrodes to the same dc potential allows one to operate the device as a long IGFET. Figure 6 shows two sets of curves. The dashed lines are the drain current versus gate voltage curves taken in a point-by-point measurement starting at low values of V_G. The electrodes were then held at a dc potential of 30 V for 90 minutes, and the measurements were repeated working from high toward low values of V_G. The strong hysteresis observed is produced by the slow time constants involved in charging the gaps to the potential of the electrodes.

Values for the carrier mobility deduced from steady-state curves obtained after the device had been sitting at a certain gate potential for a sufficiently long time are in fair agreement with measurements taken on ordinary test IGFET's with continuous gate electrodes. In both cases, the values range around 700 $cm^2\ V^{-1}\ s^{-1}$.

V. TRANSFER INEFFICIENCY

5.1 Introduction

For practically all applications of a charge-coupled device, the most crucial parameter of the device is its transfer inefficiency. Figure 7 shows some calculated output pulse trains, produced in response to the injection of single charge packets into the input of devices with different overall transfer performance. This computation was done using a linear small-signal approximation,[8] which assumes that in each transfer every charge packet leaves a fixed fraction of its charge ϵ behind, regardless of signal amplitude or the charge contained in previous stations. The overall performance of the device is suitably characterized with a "transfer inefficiency product" $n\epsilon$ multiplying the number of transfers n with the fraction of charge ϵ left behind in each transfer. Experimentally, this $n\epsilon$ product is determined by comparing the observed output pulse train with calculated model plots. For large values of $n\epsilon$ the delay of the maximum amplitude of the output pulse train is measured with respect to the calculated exit time

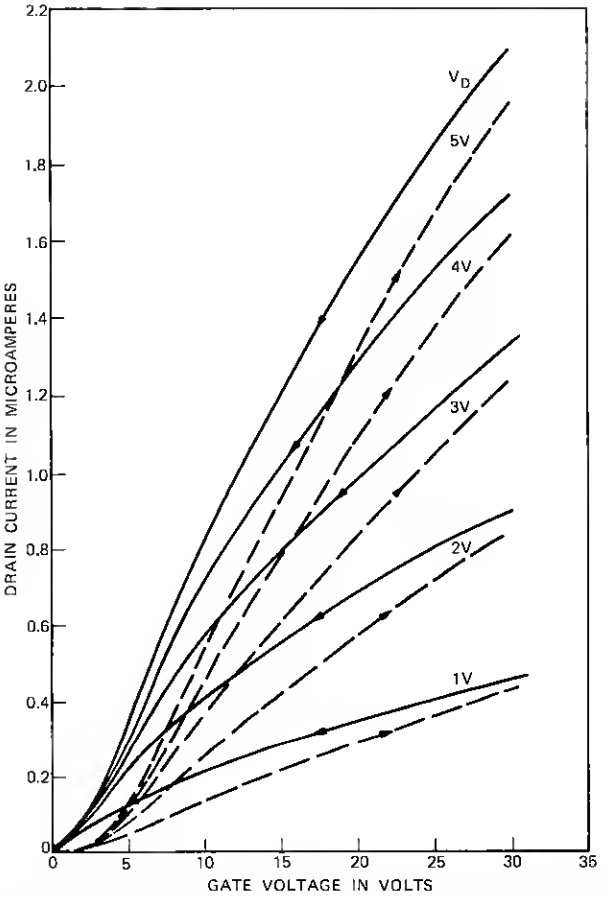

Fig. 6—Operation of the CCD as an IGFET by tying all electrodes together. Hysteresis is observed due to leakage of charge from the electrodes into the transfer gaps.

from an ideal device. This delay, expressed in a number of time slots given by the inverse of the clock frequency, is numerically equal to the transfer inefficiency product $n\epsilon$.[8]

5.2 Results

A linear model describes the actual behavior of a real device imperfectly. Small charge packets following a string of empty buckets show the biggest degradation. Figure 8 illustrates the dependence of the transfer efficiency on signal amplitude and on background charge. A

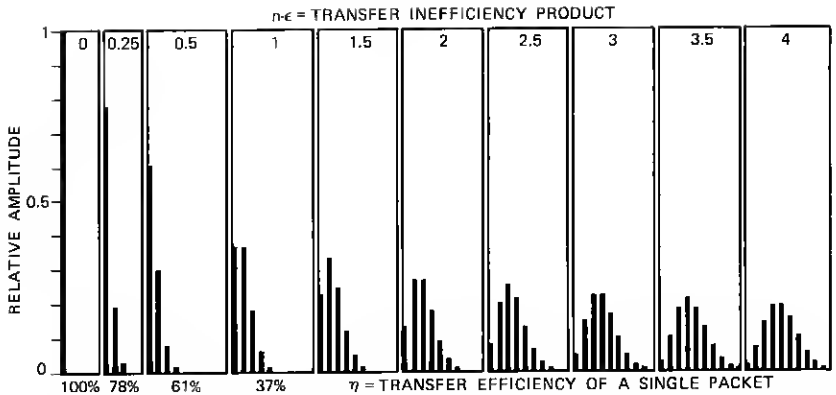

Fig. 7—Appearance of a single-charge packet at the output after transfer through a CCD with a total inefficiency product $n\epsilon$ (linear model).

sbarp spot of light with a visible diameter of about 2 μm was focused on tbe gap between two electrodes 150 transfers from tbe output end. By varying tbe integration time, the linear amplitude range of tbe device was determined. Tbe output pulse train was then monitored as a function of signal level [Fig. 8(a)]. Tbe inefficiency product decreases from 0.8 to 0.5 as tbe signal is increased from a fraction of 0.5 to 1.0 of the linear amplitude range, which was defined earlier as the saturation point. If more cbarge is injected, it can no longer be held by a single potential well. Some charge tben overflows into the neigbboring stations, forward as well as backward. In the output pulse train, some cbarge is observed to come out earlier than tbe proper time slot.

Tbe influence of background cbarge was studied by illuminating the device uniformly at various intensities. A signal charge packet corresponding to half a full well was injected witb tbe sharp light spot and tbe output monitored as a function of the amount of background cbarge [Fig. 8(b)]. Tbe infficiency product decreases from 0.8 to 0.4 as the background cbarge is increased from 0 to a fraction of 0.5 of tbe linear range. The first 20 percent of background cbarge yields the most significant improvement in performance. The measurements of Fig. 8 bave been taken at tbe clock rate of 1 MHz. The behavior is typical for frequencies below 2 MHz.

In most of tbe following experiments the transfer inefficiency was measured by using tbe device as an analog shift register. Input diode and input gate were kept at dc potentials such that the diode would just trickle a small amount of current into tbe device and thus provide some background cbarge. Every 256th clock pulse, the input diode was

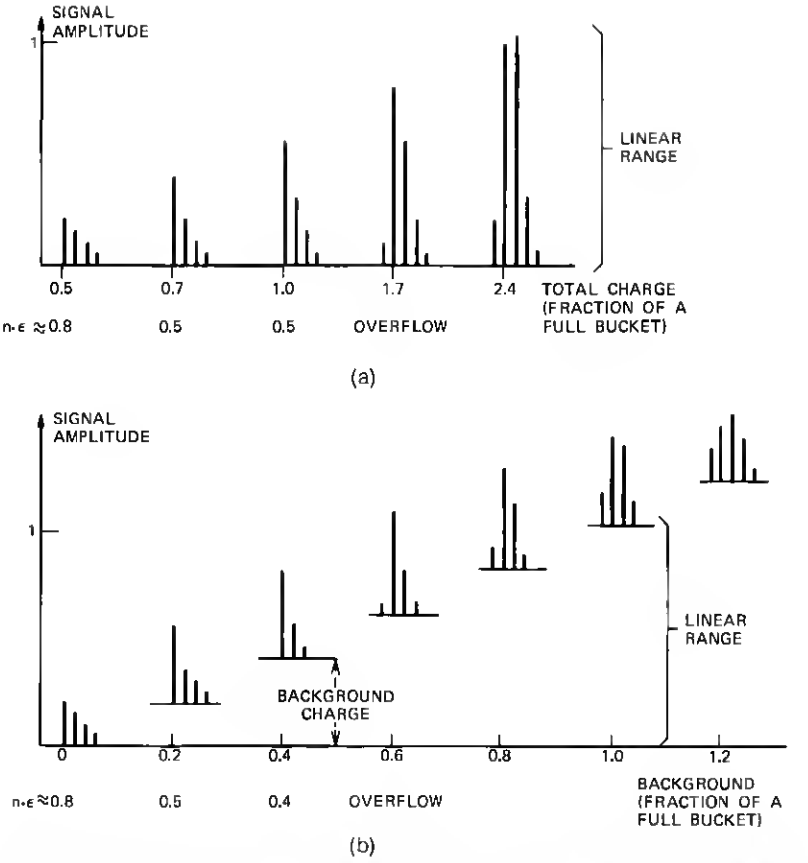

Fig. 8—Experimentally observed signal amplitudes (a) as a function of the total charge placed into one packet, (b) as a function of background charge with constant input signal charge (1 MHz).

pulsed to a more negative value for a time interval of about one-third of the clocking period and, thus, a well-defined packet of charge was injected. The charge packet was due to leave the device 500 clock pulses later. At that point, a time mark was generated that served as a reference point.

The signal from the output diode was led into a linear preamplifier consisting of a cascode stage with an active load, an emitter follower, and a current-feedback branch to the gate of the input J-FET. A set of three different amplifiers was used to cover the full range from 1 kHz to 17 MHz. The potential of the output diode was normally kept at about 10 V and the output gate at a dc potential of 2 to 5 V.

Figure 9 shows the output from two 500-element devices operated in that mode at 1 MHz. Comparison with the calculated plots in Fig. 7 shows that the two pulse trains correspond to inefficiency products of about 0.25 [Fig. 9(a)] and 3.0 [Fig. 9(b)]. However, in both cases, the tail of the pulse train extends much further than in the calculated examples. In Fig. 9(a) at least five stations carry an observable amount of charge and in Fig. 9(b) the tail extends well beyond the range of the picture. This is due to the nonlinear dependence of transfer efficiency on signal amplitude. Owing to the shape of the potential well, small packets lose a larger fraction of their charge to the following packets by trapping effects in interface states.[9] The charge packets forming the tail of the pulse train are thus transferred less and less efficiently and become more and more delayed. This nonlinear behavior is also the reason that the addition of a small amount of background charge can drastically improve the performance.

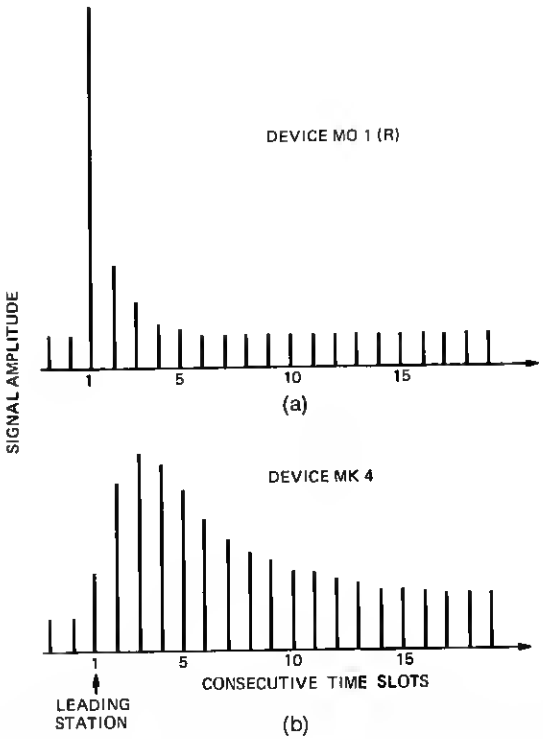

Fig. 9—Two experimentally observed signal outputs that illustrate disagreement with linear model.

The transfer efficiency of the devices studied is a sensitive function of most of such operating parameters as waveform, amplitude, and bias of the driving pulses. The dependence on signal amplitude and background charge has already been mentioned. In the following experiments, the latter two parameters were adjusted by trial and error to give the best results. Background charge ranged typically from 20 to 50 percent.

The devices are also sensitive to any changes occurring near the surface of the silicon. Some devices have shown strong sensitivity to the ambient atmosphere. Breathing slightly onto the device can change its performance considerably. A majority of the mounted devices were thus covered with a phosphorous glass to protect the bare gaps between the electrodes from the influence of the ambient. Though the sensitivity to the atmosphere could be strongly reduced by this means, the devices still showed a dependence on the history of the investigation. Prolonged operation (over one hour) at high potentials often considerably impaired the performance at lower potentials. The devices did, however, recover and resume good performance at lower potentials after they had been turned off for a few hours. These kinds of instabilities can make the experiments very tedious. To reduce their effects on the results as much as possible, the measurements have been performed first at the lower voltages and then extended to larger pulse amplitudes.

The quoted inefficiency products refer to the linear model except where otherwise stated. This seems to be justified since in the following experiments the emphasis is on the functional dependence rather than on absolute values. This approach simplifies interpretation for the reader since he can visualize that an inefficiency product $n\epsilon$ which ranges between i and $i + 1$ means that the ith station after the proper output time slot carries the maximum amount of charge.

Figure 10 shows the results of an experiment designed to demonstrate the time dependence of the performance of a device. After the device was turned off for several days, an inefficiency product of 1.8 was measured. The device was then completely flooded with current for 15 minutes by grounding the input diode while the pulses were left applied to the electrodes. The input diode was then returned to the normal condition and the performance measured at pulse amplitudes of 20 V. Figure 10 shows the strong degradation and subsequent recovery. A few seconds after the return to measurement conditions the $n\epsilon$ value was about 20 and then recovered to 2.7 within one hour and to 2.4 by the next day.

It is believed that the change in performance is due to a migration

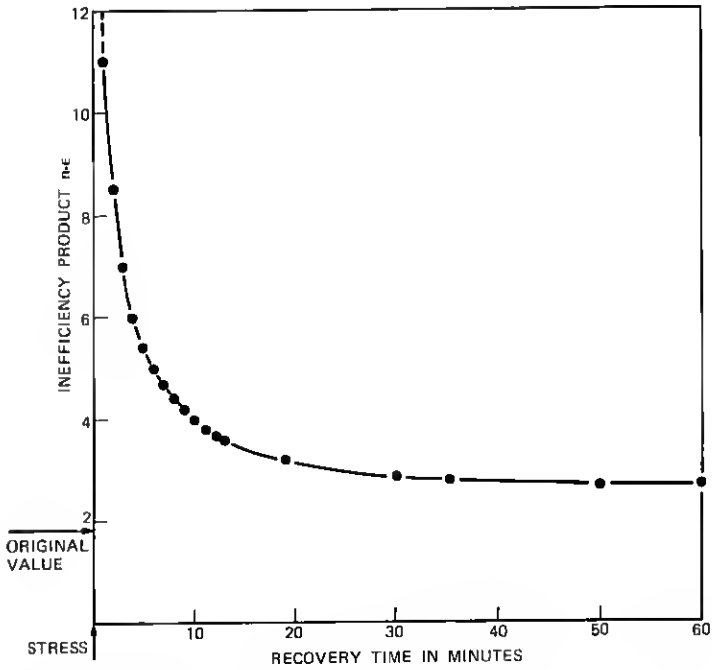

Fig. 10—Strong degradation of performance and subsequent slow recovery introduced by strong saturation of the transfer channel.

of charge at the interface between the gate dielectric and the deposited protective P glass. The excessive charge in the flooded transfer channel represents a ground plane that terminates the field lines from the transfer electrodes. Since this charge sheet extends through the whole device, it is also present under the gaps between the electrodes. Field lines from the edges of the transfer electrodes have strong lateral components that can move charge along the outer surface of the gate dielectric and, thus, charge the surface above the gaps more positively. This generates potential pockets in the silicon which can trap part of the signal charge. In normal operation of the device, the forces that charge up the gaps are absent since the charge resides under the gaps only for a fraction of a nanosecond.

The response to saturation is not equally strong in all devices. The state of the surface of the gate dielectric before the deposition of the protective P glass probably plays an important role. In the following measurements, prolonged saturation of the devices was carefully avoided.

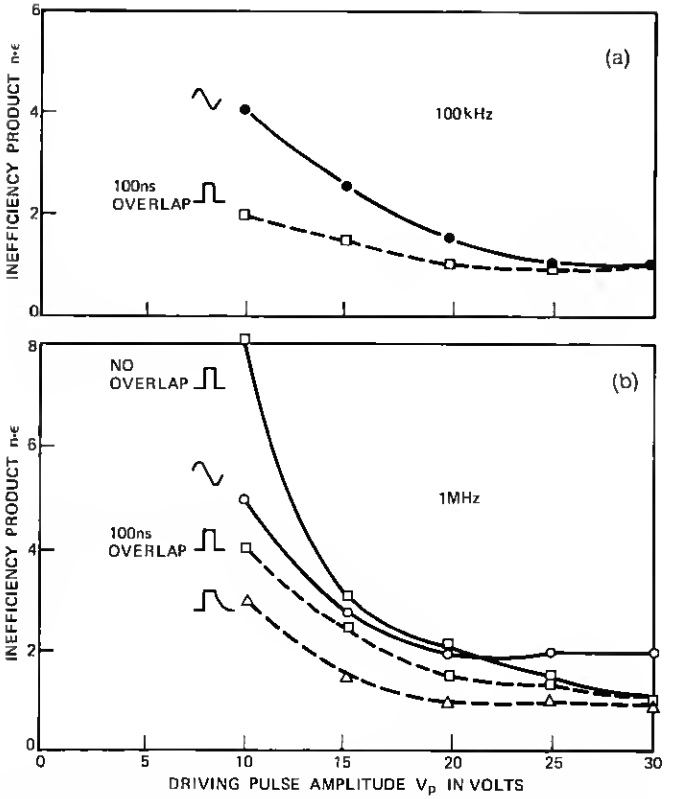

Fig. 11—Transfer inefficiency product as a function of driving pulse amplitude for various waveforms at (a) 100 kHz and (b) 1 MHz.

A set of experiments was performed to determine the best operating conditions at a given frequency. Values of $n\epsilon$ have been determined as a function of driving pulse waveforms, amplitudes, and dc bias. Figure 11 shows the dependence on waveform. At lower amplitudes, shaped square pulses with slower trailing edges give best results. For higher amplitudes, the performance is fairly independent of the driving pulse form, including sine waves.

The strong differences in the performance for the cases of square pulses of 10 V amplitude with mutual overlaps of 0 ns and 100 ns are further explored in Fig. 12. The pulses are about 300 ns long with rise and fall times of about 10 ns. The $n\epsilon$ values are measured as a function of the overlap of the driving pulses. The results are plotted in two different ways. In Fig. 12(a) the overlap in time cor-

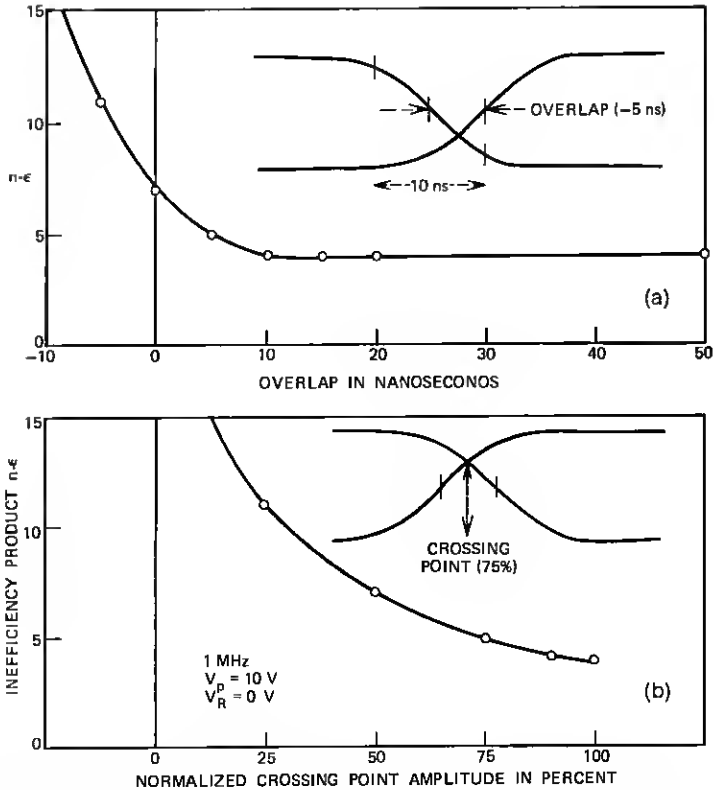

Fig. 12—Transfer inefficiency product as a function of mutual overlap for square driving pulses plotted in two different ways (see inset for definitions).

responding to the 50-percent point of the waveforms is measured in nanoseconds. A negative overlap thus means that the waves cross at less than 50 percent of their peak values. The hest performance is reached for overlaps of more than 10 ns. Figure 12(h) shows the same results plotted as a function of the amplitude at the crossing point. The hest performance is reached for a crossing point higher than 90 percent of peak amplitude, which corresponds to overlaps of more than 10 ns.

Square pulses with 10-ns overlap have heen used to evaluate the influence of the resting potential on the performance. In Fig. 13(a), the dependence on pulse amplitude is first estahlished. For pulse amplitudes higher than ahout 10 V, which seem to he necessary to override some harrier in the hare gaps, performance improves slowly hut

monotonically toward higher amplitudes. For a pulse amplitude of 15 V, the influence of the resting potential V_R was studied [Fig 13(b)]. The device is operable in a range of V_R up to about 10 V with the best performance near 6 V. Again, it has to be pointed out that such a wide operating range has not been observed too often.

In these conditions in which there are square pulses with 10-ns overlap, the transfer efficiency was measured for clock rates between 1 kHz and 17 MHz. At each frequency, the amount of background charge and the signal level were adjusted to give the best results. Background charge ranged from 15 to 30 percent and signal amplitudes from 30 to 50 percent of a full bucket. The devices were operated as shift registers in the continuous wave mode. Single charge packets were injected every 256 clock pulses. Over more than three orders of magnitude from 1

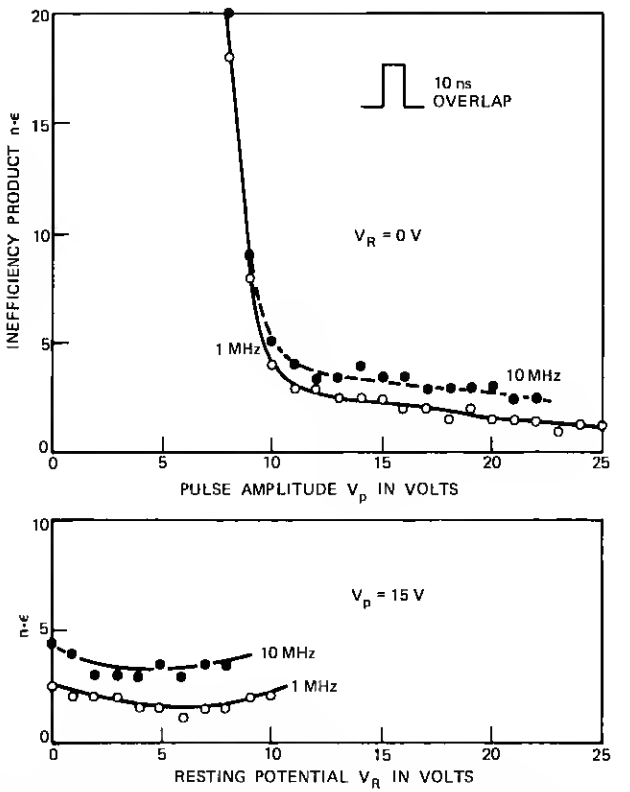

Fig. 13—Transfer inefficiency product as a function of (a) pulse amplitude and (b) resting potential for clock frequencies of 1 MHz and 10 MHz.

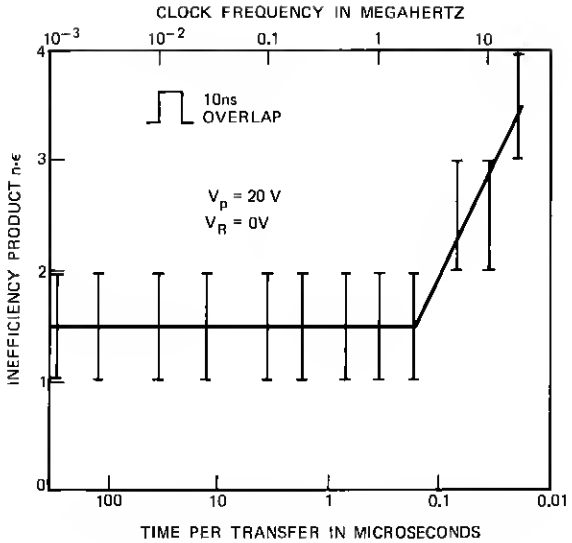

Fig. 14—Transfer inefficiency product as a function of clock frequency or available transfer time.

kHz to 2 MHz no significant differences in performance were measurable (Fig. 14). Then, from 2 MHz to 17 MHz the $n\epsilon$ value rose from about 1.5 to 3.5. This decrease in performance does not stem from the free-charge-transfer mechanism itself. The time available per transfer, even at the highest frequency where it is 20 ns, is still long compared to the calculated transfer time constants, which are well below 1 ns.[6] An increase in the interface state density toward the conduction band edge could account for the decrease in performance at the highest frequencies.[9] Furthermore, above 5 MHz, the driving pulses as observed on the connector to the device were far from perfect, and additional degradation might have heen produced by stray capacitance and by the diffused crossunders on the device itself.

5.3 Discussion

To study the transfer performance of a CCD, an optimum numher of transfers exist, depending upon the performance of the device. If the device is too short, the degradation is too small to be measured accurately. If the device is too long, the degradation is large and, thus, again $n\epsilon$ is difficult to measure accurately. Values of $n\epsilon$ on the order of one are most easily measured.

For long devices another problem arises. The measured functional dependences might be smeared due to nonuniformities of some physical parameters along the transfer channel, such as flat-hand voltage or electrode width. Figure 15 illustrates the integrated $n\epsilon$ values measured with a spot of light injected at various distances from the output diode. It can be seen that $n\epsilon$ is not linearly increasing along the device. In some other devices, sharp steps in the $n\epsilon$ curves have heen observed which often could be correlated with an obvious physical defect, such as a partly missing transfer electrode.

The observed inefficiency products ranged from 0.2 to several hundred. They are distributed in a log-normal manner around a value of 20 with a standard deviation of about a factor of five. This spread is too high to be explained hy variations in interface state densities. These devices are, however, very sensitive to variations in the fixed oxide charge in the transfer gaps. Too little or too much charge can lead to barriers or pockets in the interface potential, both of which strongly impair the transfer efficiency of the device. These effects associated with the transfer gaps are strong enough to override other parameters

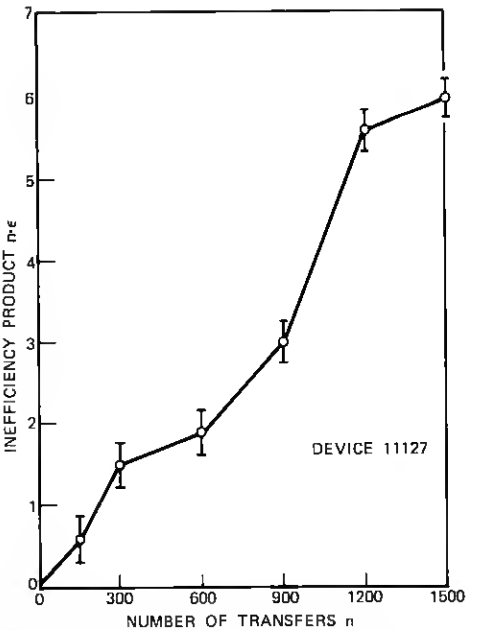

Fig. 15—Transfer inefficiency product from various points of the device to the output. The charge was injected with a light spot.

that could influence the measured inefficiency products. A survey of the storage times of MOS capacitors, of the average dark currents of working devices, and of their $n\epsilon$ values was performed on 35 slices in dynamic prohe tests; although the ohserved values for the storage times and for the dark currents correlated reasonahly well from slice to slice, no correlation between $n\epsilon$ and either of the other two measurements could he found.

The hest results observed are $n\epsilon = 0.2$, which corresponds to $\epsilon = 1.3 \times 10^{-4}$, a value comparahle to results reported on 2-phase devices.[10,11] Values hetween 10^{-4} and 10^{-3} can he expected with interface states densities in the low 10^{10} cm^{-2} eV^{-1}.[9] The majority of devices, however, have ϵ values hetween 10^{-3} and 10^{-2}. These values lie in the range of what has heen ohtained with ordinary bucket-brigade devices.[12,13] This similarity leads to the suggestion that gapped devices often work in a similar mode. Fixed harriers in the gaps keep a reservoir of carriers underneath each electrode. The signal charge modulates the harrier height, and transfer efficiencies comparahle to hucket-hrigade structures can he expected.

VI. DARK CURRENT

When the linear CCD is used as a line imaging device, one set of electrodes is switched to an integration potential V_I during the time that charge is heing integrated. The minority carriers generated hy the incoming light are then collected hy the potential wells underneath that set of electrodes. After a sufficient charge pattern has heen accumulated, the stored information is read out in serial form.

In the ahsence of any illumination, minority carriers are still generated hy thermal effects and are collected in the nearest potential wells. The generation rate is not necessarily uniform over the whole device and, thus, this dark current can generate a pattern of its own. Figure 16 shows the readout signal of a fairly nonuniform device after integration times of 250 ms and 500 ms where in the latter case the highest peaks of the signal have already reached saturation. During readout each charge packet picks up a little hit of dark current from all the locations it passes on its way to the output diode. From all the other locations on the input end of the device, it had already received a dark current contrihution during the readout of the previous line when the "empty" packet was moved from the input diode to the integration site. Therefore, the same integral contrihution is added to every charge packet. This uniform component can be subtracted or, if the

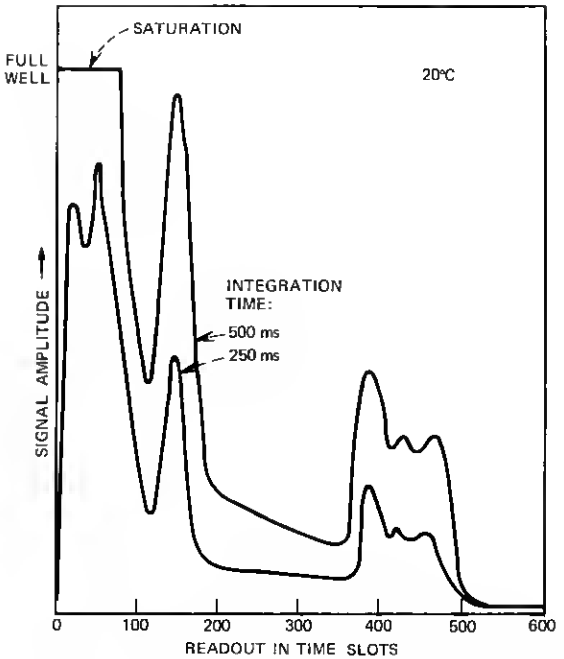

Fig. 16—Integrated dark current profile for two different integration times.

readout time is kept short compared to the integration time, it can be neglected.

For low-light-level-imaging applications, the dark current should be as low as possible. Cooling the device is a possible means to reduce the thermal carrier generation. For a simple demonstration the device was mounted on an open cooling block. Figure 17 shows the results for a temperature interval from −20°C to +60°C. As expected, the inefficiency product showed no significant changes except below −15°C where the formation of ice degraded the operation of the device. The dark current measurements displayed in Fig. 17 were taken near element 150 in the signal shown in Fig. 16. Within the measurement accuracy they follow the calculated dependence given by the intrinsic carrier density n_i.

There are mainly two mechanisms that produce a dark current component which is proportional to n_i.[14,15] The generation current arising from bulk states in a 5-μm-wide depletion region is on the order of 6 nA/cm^2 for a minority carrier lifetime of 100 μs, which typically

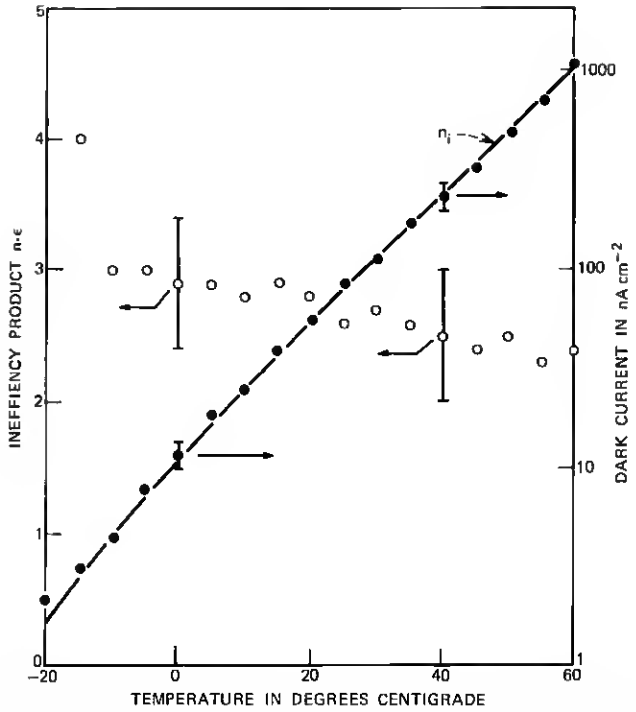

Fig. 17—Measured inefficiency products (left ordinate) and local dark current generation (right ordinate) compared to temperature dependence of intrinsic carrier density n_i (matched at 20°C).

can he expected in a good sample. The generation current arising from interface states with an estimated density of $2 \times 10^{10}/\text{cm}^2/\text{eV}$ at midband is on the order of 4.6 nA/cm². Thus, surface and hulk dark current contrihutions are of the same order of magnitude. The shape of the thermal relaxation curve of the MOS capacitor can he analyzed to determine which is the dominant component in a particular sample.[16] In a CCD the situation is complicated hy the fact that the two components normally do not have the same active generation area. While the strong depletion region is mainly localized underneath one electrode per element only, a small depletion region extends underneath all electrodes and thus the surface contribution stems from an area that is several times larger.

Several devices showed a fairly uniform dark current hackground on the order of 10 nA/cm², hut superposed hy highly localized point defects. The temperature dependence of some of these localized

generation centers does not show the simple proportionality with n_i, hut has a range of weaker temperature dependences. At a given temperature, the number of ohservahle current sources as well as their strength depends strongly on the electric field, i.e., on the potential V_I applied to the integrating electrode set. Most defects seem to fill the integrating potential well and then stop their activity as would be expected from states that are only active in the depleted hulk of the silicon suhstrate. Other defects, however, possihly located at the interface, continue to generate minority carriers and fill adjacent wells and eventually a whole transfer channel. These ohservations indicate that there is a variety of localized defects.

VII. LIGHT SENSITIVITY

The described device can he used in slow-scan-imaging applications as a simple line scanner that integrates the information incident upon the transfer region itself. The transfer electrodes are opaque and, thus, ahout 50 percent of the light incident on the transfer region is lost. The resolution of such a system in the direction of the electronic scan has heen discussed elsewhere[17] and experimental results presented.[4] The resolution in the direction of the mechanical scan depends on the effective light-collecting line width of the device. This width has heen measured by prohing the device with a very narrow spot of light (approximately 2 μm wide) produced hy an incandescent hulh from which the IR radiation has heen filtered out. This spot was moved along two different lines across the transfer channel of the device (see Fig. 18). Line A lies heside one of the integrating electrodes, and the generated charge, thus, will spill mainly into the potential well underneath. Carriers generated deep down in the hulk can reach adjacent wells hy diffusion. To measure the total amount of charge, the signals of the two adjacent stations were added to the main station. To eliminate effects of transfer inefficiency, the experiment was performed close to the output diode.

In a second experiment, the spot of light was moved along line B lying midway hetween two integrating electrodes. The charge was then distrihuted more or less equally into the two potential wells and the sum of the two signals was used in plotting Fig. 18.

Both experiments yield the same sensitivity across the channel. The 50-percent point is ahout 10 μm outside the edge of the transfer channel, indicating that the channel stopping diffusion does not provide adequate definition of the optical integration region. The equivalent line width of this image sensor is, thus, 35 μm or ahout twice as large as

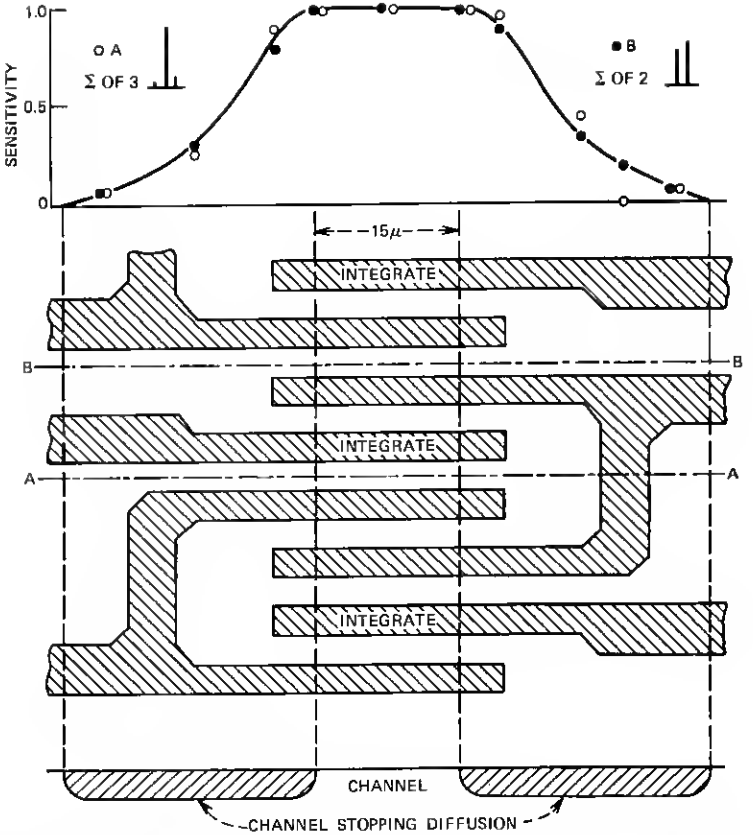

Fig. 18—Normalized light sensitivity measured with a narrow light spot in two different traces across the transfer channel.

the length of a CCD element. Such a device should, therefore, give a much better resolution in the direction of the electronic scan than in the direction of the mechanical scan. This agrees with experimental observations. To improve the vertical resolution of this imaging system to match the horizontal resolution, the light-sensitive line width would have to be confined to about half the element length.

VIII. VARIATIONS IN TECHNOLOGY

Devices with different insulator thickness, electrode length, and metallization have been built to study the influence of these parameters on device behavior. While the effect on signal-handling ability followed a predictable pattern, the influence on transfer inefficiency was often

concealed by the large spread of the observed values. Still some trends became evident.

If operated at the same potentials, a thinner insulator leads generally to a higher signal-handling ability, as expected from the higher capacitance. When the operating voltages are lowered proportionally to the reduced insulator thickness, the devices show poor performance. High potential differences between adjacent transfer electrodes are still necessary to produce fringe fields that can overcome the fixed potential barriers in the gap. With a thinner insulator, the dependence on V_R becomes more critical, and the devices show a narrower operating range. This trend can be compensated for if, at the same time, the gaps are narrowed. With an oxide thickness of 1500 Å, 2 μm seemed to be an appropriate gap width to achieve an average operating range for V_R on the order of 1 V. No significant change in behavior could be attributed to the replacement of 1500 Å of SiO_2 with a double insulator structure consisting of 1200 Å SiO_2 and 500 Å Al_2O_3.

Three different metallizations have been compared: W, Al, Ti-Pd-Ni. No specific difference in performance was observed in devices with chemically etched W or Al electrodes. On devices with a Ti-Pd-Ni metallization on a SiO_2-Al_2O_3 insulator a backsputtering process[7] was used to obtain the required accuracy in the delineation of the transfer electrodes. Figure 19 compares the results of the dynamic probe tests on all operating backsputter delineated devices with a control batch with chemically etched electrodes on the same double insulator. The backsputtered devices showed n_ϵ values that were on the average about a factor of six higher than the values obtained on devices with W or Al electrodes. Among possible causes, differences in the interface state density underneath the electrodes and variations in gap width due to a possible undercutting of the Ti have been ruled out experimentally. Thus, it is conjectured that the backsputter process degrades the integrity of the Si-SiO_2 interface in the region of the gaps where the metal is thinned to within 1000 Å of the insulator surface during backsputtering.[18] In spite of the wide spread of values, this particular trend in n_ϵ was clearly visible, because its origin itself is associated with the transfer gaps, which are the single most significant cause for high transfer inefficiency.

To reduce the sensitivity to the ambient, some slices were protected with a dielectric level of, for example, 1 μm of phosphorous glass or 1000 Å of silicon nitride. While the reaction to such simple tests as "breathing onto the device" was strongly reduced, transfer efficiency did not improve on the average, nor did the slow instabilities disappear.

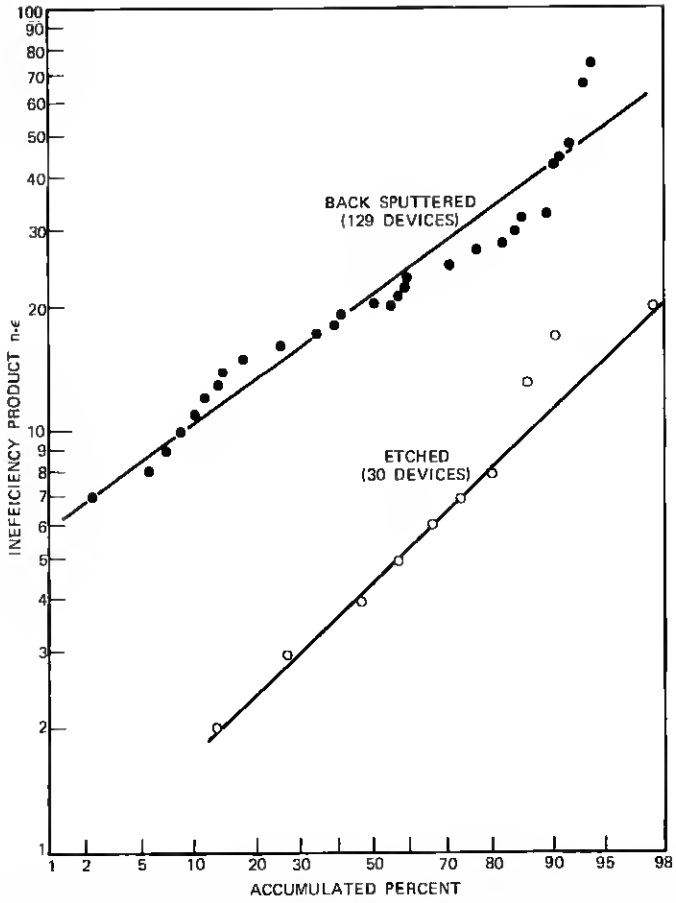

Fig. 19—Plot of $n\epsilon$ distribution for all operating backsputter delineated devices and for a control batch with etched electrodes.

The results generally leave the impression that the condition of the surface of the gate insulator in the gaps during the deposition of the protective dielectric is crucial to the final performance of the device.

In another attempt to control the potential in the gaps, six finished devices with 1500 Å of SiO_2 and 3 μm gaps, which orginally operated with $n\epsilon$ products of 5 to 10, were overcoated with a strip of polycrystalline silicon, with sheet resistances ranging from 10^8 to 10^{10} ohms/square. In two cases the $n\epsilon$ product improved to values around two and in one case even below one. The performance of the other

three devices worsened and showed some erratic behavior. Still, these results suggest that a properly developed resistive sea might possibly yield a solution to the gap problem.

IX. SUMMARY

Signal-handling ability, transfer efficiency, and dark-current profiles of over a hundred individual linear CCD's have been studied. The total spread of the result is surprisingly wide. Many erratic effects have been observed but not investigated in detail and, therefore, are not fully understood. On several devices which showed reasonably good performance and no erratic behavior, a thorough investigation of the functional dependence of the performance on various parameters has been carried out. These dependences are well understood and can be explained with simple models. Deviations from these simple models as well as the limitations in performance seem to be mainly associated with the gaps between the transfer electrodes. Poorly controlled surface potential can lead to the formation of barriers or pockets that produce poor transfer efficiency, slow instabilities, and nonuniformities in large devices.

Three-phase CCD's with gaps between the electrodes have been an invaluable tool for the investigation of charge coupling and for an early demonstration of charge-coupled image sensors. But the technologies presently used to make these structures do not produce reliable devices with consistent performance. With some technological effort a solution to the gap problem can probably be found, for instance in the application of a resistive sea on the surface of the device. It is questionable, however, if it is worthwhile to put such a development effort into this structure. In big devices the large number of narrow gaps cause a serious reduction in yield. Furthermore, the peripheral structures in more complex devices might require more than one level of metallization. It seems more advantageous to build the actual CCD with overlapping gates and to provide a completely sealed channel.

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REFERENCES

1. W. S. Boyle and G. E. Smith, "Charge-Coupled Semiconductor Devices," B.S.T.J., *49*, No. 4 (April 1970), pp. 587–593.
2. M. F. Tompsett, G. F. Amelio, and G. E. Smith, "Charge-Coupled 8-bit Shift Register," Appl. Phys. Lett., *17*, 1970, pp. 111–115.
3. M. F. Tompsett, G. F. Amelio, W. J. Bertram, R. R. Buckley, W. J. McNamara, J. C. Mikkelsen, and D. A. Sealer, "Charge-Coupled Imaging Devices: Experimental Results," IEEE Trans. Electron. Devices, *ED-18*, 1971, pp. 992–996.
4. W. J. Bertram, D. A. Sealer, C. H. Séquin, and M. F. Tompsett, "Recent Advances in Charge-Coupled Imaging Devices," IEEE INTERCON Digest of Papers, 1972, pp. 292–293.
5. M. F. Tompsett and E. J. Zimany, "Use of Charge-Coupled Devices for Analog Delay," IEEE Jour. Solid-State Circuit, *SC-8*, 1973, pp. 151–157.
6. G. F. Amelio, "Computer Modeling of Charge-Coupled Device Characteristics," B.S.T.J., *51*, No. 3 (March 1972), pp. 705–730.
7. E. F. Lahuda, to be published.
8. W. B. Joyce and W. J. Bertram, "Linearized Dispersion Relation and Green's Function for Discrete-Charge-Transfer Devices with Incomplete Transfer," B.S.T.J., *50*, No. 6 (July-August 1971), pp. 1741–1759.
9. M. F. Tompsett, "The Quantitative Effects of Interface States on the Performance of CCDs," IEEE Transactions on Electron Devices, *ED-20*, 1973, pp. 45–55.
10. W. F. Kosonocky and J. E. Carnes, reported at the ISSCC in Philadelphia, February 17, 1972.
11. N. A. Patrin, A. Bhattacharyya, M. L. Joshi, and J. J. Chang, "Memory Potential of CCD," Nerem 82 Record, 1972, pp. 157–160.
12. L. Boonstra and F. L. J. Sangster, "Progress on Bucket-Brigade Charge Transfer Devices," reported at the ISSCC in Philadelphia, February 17, 1972.
13. C. N. Berglund and H. J. Boll, "Performance Limitations of the IGFET Bucket-Brigade Shift Register," IEEE Trans. Electron Devices, *ED-19*, 1972, pp. 852–860.
14. See, for example, A. J. Grove, *Physics and Technology of Semiconductor Devices*, New York: Wiley, 1967, pp. 298–302.
15. G. F. Amelio, W. J. Bertram, and M. F. Tompsett, "Charge Coupled Imaging Devices: Design Considerations," IEEE Trans. Electron Devices, *ED-18*, 1971, pp. 986–992.
16. F. P. Heiman, "On the Determination of Minority Carrier Lifetime from the Transient Response of an MOS Capacitor," IEEE Trans. Electron Devices, *ED-14*, 1967, pp. 781–784.
17. C. H. Séquin, "Interlacing in Charge-Coupled Imaging Devices," IEEE Trans. Electron Devices, *ED-20*, 1973.
18. B. B. Kosicki, private communication.